What is claimed is:

[Claim 1] 1. A method for grain size determination, the method comprising the steps of:

(a) providing an electrically conducting line including N sections of equal length, wherein N is an integer greater than 1;
(b) measuring N electrical resistances respectively corresponding to the N sections;
(c) determining a number of grains in the line based on the N measured electrical resistances of the N sections; and
(d) determining an average grain size of the line based on a length of the line and the number of grains in the line.

[Claim 2] 2. The method of claim 1, wherein the step (c) comprises the steps of:

determining a number of grain boundaries in each section of the N sections of the line based on the N measured electrical resistances of the N sections;

determining a total number of grain boundaries in the line based on the number of grain boundaries in each section of the N sections of the line; and

determining the number of grains in the line based on the total number of grain boundaries in the line.

[Claim 3] 3. The method of claim 2, wherein the step of determining the number of grain boundaries in each section of the N sections of the line based on the N measured electrical resistances of the N sections comprises the steps of:

grouping the N measured electrical resistances of the N sections into M groups of similar electrical resistances, wherein M is an integer greater than or equal to 1 but less than N;

identifying a first group of the M groups that contain the lowest, similar electrical resistances, a second group of the M groups that contain the next-

higher, similar electrical resistances,..., and an M^{th} group that contain the highest, similar electrical resistances;

determining a number of grain boundaries for each group of the M groups, wherein the number of grain boundaries for the group represents the number of grain boundaries in a section of the N sections whose associated electrical resistance is in the group; and

determining the number of grain boundaries in each section of the N sections based on the number of grain boundaries for the group that contains the electrical resistance of the section.

[Claim 4] 4. The method of claim 3, wherein the step of determining the number of grain boundaries for each group of the M groups comprises the step of determining that the number of grain boundaries for the first group is zero.

[Claim 5] 5. The method of claim 2, wherein the step of determining the number of grains in the line based on the total number of grain boundaries in the line comprises the step of adding one to the total number of grain boundaries in the line to obtain the number of grains in the line.

[Claim 6] 6. The method of claim 1, further comprising the steps of determining that a chip that contains the line is defective if the average grain size of the line is not within a pre-specified range.

[Claim 7] 7. A method of line evaluation, comprising the steps of:

(a) providing a line evaluation structure comprising N electrically conducting lines,

wherein N is a positive integer,

wherein, for $i = 1,2,...,N$, the i^{th} line of the N electrically conducting lines comprises M_i line sections, M_i being a positive integer, such that the N electrically conducting lines comprise in total S line sections, wherein $S = \Sigma M_i$ $(i = 1,2,...,N)$,

wherein each line section of the S line sections is of the same length, and

(b) measuring electrical resistance of each line section of the S line sections; and

(c) determining a line geometry adjustment for the line evaluation structure based on the electrical resistances of the S line sections obtained in step (b),

wherein the line geometry adjustment represents an effective reduction of cross-section size of the N electrically conducting lines as a result of grain boundary electrical resistance.

[Claim 8] 8. The method of claim 7, wherein the step of determining the line geometry adjustment comprises the steps of:

identifying a first group of sections of the S line sections that have no grain boundary;

identifying a second group of sections of the S line sections that have only one grain boundary;

determining a first average electrical resistance for the first group and a second average electrical resistance for the second group;

determining an average grain boundary electrical resistance as the difference between the second average electrical resistance and the first average electrical resistance; and

determining the line geometry adjustment based on the average grain boundary electrical resistance.

[Claim 9] 9. The method of claim 8, wherein the step of identifying the first group of sections of the S line sections that have no grain boundary comprises the steps of:

identifying similar, lowest values of the electrical resistances of the S line sections; and

identifying sections of the S line sections associated with the identified similar, lowest values of the electrical resistances as the first group of sections.

[Claim 10] 10. The method of claim 8, wherein the step of identifying the second group of sections of the S line sections that have only one grain boundary comprises the steps of:

identifying similar, next-to-lowest values of the electrical resistances of the S line sections; and

identifying sections of the S line sections associated with the identified similar, next-to-lowest values of the electrical resistances as the second group of sections.

[Claim 11] 11. The method of claim 8, wherein the step of determining the line geometry adjustment based on the average grain boundary electrical resistance comprises the step of extracting the line geometry adjustment from the equation $R(\text{no GB})/Rb(\text{one GB}) = (w - \epsilon)*(h - \epsilon)/(w*h)$,

wherein R(no GB) is the first average electrical resistance for the first group,
wherein Rb(one GB) is the second average electrical resistance for the second group,
wherein w is a line width of a line of the N electrically conducting lines, and
wherein h is a thickness of a line of the N electrically conducting lines.

[Claim 12] 12. The method of claim 11, wherein w is a line width that is close to but does not exceed an average grain size of the N electrically conducting lines.

[Claim 13] 13. The method of claim 7, further comprising the step of determining a chip containing the line evaluation structure as defective if the line geometry adjustment exceeds a pre-specified value.

[Claim 14] 14. A method of line evaluation, comprising the steps of:

(a) providing a line evaluation structure comprising N electrically conducting lines of a same length and a same thickness,

wherein N is a positive integer,

wherein the N electrically conducting lines have M different line widths,
wherein M is a positive integer and $M \leq N$, and
wherein each line of the N electrically conducting lines is configured to be measured for electrical resistance;
(b) for each temperature of P different temperatures and for each line width of the M line widths, measuring an electrical resistance for the line width at the temperature, wherein P is an integer greater than 1;

(c) for each line width of the M line widths, determining a temperature coefficient of electrical resistance (TCR) based on the P electrical resistances at P temperatures for the line width;
(d) determining first and second line geometry adjustments for the N electrically conducting lines based on the M TCRs of the M line widths determined in step (c),

wherein the first line geometry adjustment represents an effective reduction of line width of the N electrically conducting lines as a result of grain boundary electrical resistance and sidewall surface roughness of the N electrically conducting lines, and

wherein the second line geometry adjustment represents an effective reduction of thickness of the N electrically conducting lines as a result of grain boundary electrical resistance and top/bottom surface roughness of the N electrically conducting lines.

[Claim 15] 15. The method of claim 14, wherein the step (c) comprises the steps of:

curve-fitting a straight line to P points for the P temperatures, wherein each point of the P points represents a temperature of the P temperatures and the associated electrical resistance for the line width at the temperature; and

determining the TCR for the line width based on the resulting straight line.

[Claim 16] 16. The method of claim 15, wherein the straight line has a formula of $R = Ro*[1 + TCR*(T - To)]$, wherein T is temperature variable, R is electrical resistance variable for the line width, TCR is the temperature coefficient of electrical resistance of the line width at (To,Ro), and (To,Ro) is a point on the straight line.

[Claim 17] 17. The method of claim 14, wherein the step (d) comprises the steps of:

curve-fitting a curve to M points for the M line widths on an orthogonal x-y axis system, wherein each point of the M points represents a line width of the M line widths and the associated TCR for the line width; and

determining the first and second line geometry adjustments for the N electrically conducting lines based on the curve.

[Claim 18] 18. The method of claim 17, wherein the curve has a formula of $TCR = TCRo*(W - \delta)*(H - \theta)/(W*H)$,

wherein TCR is a variable of temperature coefficient of electrical resistance,
wherein TCRo is the bulk TCR of a material of the N electrically conducting lines,
wherein W is the line width variable associated with TCR,
wherein H is the thickness of the N electrically conducting lines, and
wherein δ and θ are the first and second line geometry adjustments, respectively.

[Claim 19] 19. The method of claim 14, further comprising the steps of:

determining a third line geometry adjustment based on the first line geometry adjustment,
wherein the third line geometry adjustment represents an effective reduction of line width of the N electrically conducting lines as a result of sidewall surface roughness of the N electrically conducting lines; and

determining a fourth line geometry adjustment based on the second line geometry adjustment,
wherein the fourth line geometry adjustment represents an effective reduction of thickness of the N electrically conducting lines as a result of top/bottom surface roughness of the N electrically conducting lines.

[Claim 20] 20. The method of claim 19, further comprising the step of determining a chip containing the line evaluation structure as defective if either of the second and third line geometry adjustments exceeds its respective pre-specified value.